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SESSION: RF CMOS building blocks table of contents
Pages: 286 - 291
Year of Publication: 2006
ISBN:1-59593-462-6

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Sponsors
ACM: Association for Computing Machinery
SIGDA: ACM Special Interest Group on Design Automation

Publisher ACM New York, NY, USA

ABSTRACT

A CMOS divider concept without static power consumption, except leakage power, is proposed. The circuit divides an input signal by two and generates four phases with highly accurate phase skew of 90 degrees. In a 90nm low-power CMOS technology, the maximum operation frequency is 11.6 GHz for a supply voltage of 1.5V slow process and worst case operation parameters. Higher frequencies can be achieved by a hybrid approach where the signal is first divided by a factor of two in a single CML stage and then by the proposed circuit by another factor of two for the generation of the four phases. The divider is applied to dual modulus pre-

scalers and IQ receivers. A variant of the circuit contains an intrinsic phase-rotator, so the power consumption of the pre-scaler is not only reduced due to the logic style but also by a simplified architecture of the overall pre-scaler.

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INDEX TERMS

Primary Classification:
B. Hardware
B.4 INPUT/OUTPUT AND DATA COMMUNICATIONS
B.4.1 Data Communications Devices

General Terms:
Design

Keywords:
divider, low-power, phase-rotator, pre-scaler

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